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EXAMINER
SHAPIRO, LEONID

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 01/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/747,194	YOKOYAMA, RYOICHI	
	Examiner	Art Unit	
	Leonid Shapiro	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 May 2004 and 02 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) *1-9,11 and 40-49* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10, 12-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Election/Restrictions

1. Applicant's election without traverse of claims 10 and 12-39 in the reply filed on 05.18.04 is acknowledged.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 10, 12-13, 16-17, 20-23, 25-26, 34-35, 37-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al. (US Patent 5,945,972) in view of Akiyama et al. (US Patent 5,977,940).

As to claim 10, Okumura teaches a display apparatus comprising:

a plurality of gate lines provided in one direction of a substrate (See Fig. 2B, items La1, La2..., Col. 12, Lines 52-53);

a plurality of drain lines provided in a direction intersecting with gate lines (See Fig. 2B, items Lb1, Lb2..., Col. 12, Lines 52-53); and

a plurality of display pixels, each of which is selected by a scan signal supplied from corresponding one of plurality of gate lines, and which is supplied with an image signal from corresponding one of plurality of drain lines (See Fig. 2B, items La1, La2,..., Lb1, Lb2...); wherein

each of plurality of display pixels comprises:

a display element (See Fig. 2B, 3, item CEL, Col. 13, Lines 16-24);

a first display circuit having a storing circuit, for storing a digital image signal from corresponding one of plurality of drain lines in response to a scan signal from corresponding one of gate lines (See Fig. 2B, 3, items Lai, Lbj, Col. 13, Lines 39-49), and a signal selector which is operated based on data stored at storing circuit (See Fig. 4A, item OBJ, Col. 14, Lines 53-57) for selecting an output signal from among two or more display signals and for supplying selected signal to display element (See Fig. 5, items 121a-121m, 123', Col. 13, Lines 28-38);

wherein display pixel further comprises a display circuit selector (See Fig. 3, item 123) for selectively supplying an image signal from corresponding one of drain lines (See Fig. 3, item Lbj) to the first (See Fig. 3, item 121a) or second display circuit (See Fig. 3, item 121b, Col. 14, Lines 7-54).

Okumura et al. teaches the display signal may be stored in the first memory circuit in the either digital or analog form (See Fig. 27, items 532, 535, in description See Col. 27, lines 10-14 and Lines 51-55).

Okumura et al. does not show a second display circuit having a storage capacitor for storing an analog image signal from corresponding one of drain lines in response to a scan signal from corresponding one of gate lines, wherein the signal stored in storage capacitor is supplied to display element.

Akiyama et al. teaches display circuit having a storage capacitor for storing an analog image signal from corresponding one of drain lines in response to a scan signal from corresponding one of gate lines, wherein the signal stored in storage capacitor is

supplied to display element (See Fig. 1A, items 2, 5, 8, from Col. 9, Line 38 to Col. 10, Line 35).

It would have been obvious to one ordinary skill in the art at time of the invention to incorporate teaching of Akiyama et al. into Okumura et al. system in order to reduce the power consumption (See Col. 3, Lines 23-29).

As to claim 12, Okumura teaches a display apparatus comprising:

a plurality of gate lines provided in one direction of a substrate (See Fig. 2B, items La1, La2..., Col. 12, Lines 52-53);

a plurality of drain lines provided in a direction intersecting with gate lines (See Fig. 2B, items Lb1, Lb2..., Col. 12, Lines 52-53); and

a plurality of display pixels, each of which is selected by a scan signal supplied from corresponding one of plurality of gate lines, and which is supplied with an image signal from corresponding one of plurality of drain lines (See Fig. 2B, items La1, La2..., Lb1, Lb2,...); wherein

each of plurality of display pixels comprises:

a display element (See Fig. 2B, 3, item CEL, Col. 13, Lines 16-24);

a first display circuit having a storing circuit, for storing a digital image signal from corresponding one of plurality of drain lines in response to a scan signal from corresponding one of gate lines (See Fig. 2B, 3, items Lai, Lbj, Col. 13, Lines 39-49), and a signal selector which is operated based on data stored at storing circuit (See Fig. 4A, item OBJ, Col. 14, Lines 53-57) for selecting an output signal from among two or

more display signals and for supplying selected signal to display element (See Fig. 5, items 121a-121m, 123', Col. 13, Lines 28-38);

wherein display pixel further comprises a data selector (See Fig. 3, item 123) for selectively supplying an image signal from corresponding one of drain lines (See Fig. 3, item Lbj) to the first (See Fig. 3, item 121a) or second display circuit (See Fig. 3, item 121b, Col. 14, Lines 7-54).

Okumura et al. teaches the display signal may be stored in the first memory circuit in the either digital or analog form (See Fig. 27, items 532, 535, in description See Col. 27, lines 10-14 and Lines 51-55).

Okumura et al. does not show a second display circuit having a storage capacitor for storing an analog image signal from corresponding one of drain lines in response to a scan signal from corresponding one of gate lines, wherein the signal stored in storage capacitor is supplied to display element.

Akiyama et al. teaches display circuit having a storage capacitor for storing an analog image signal from corresponding one of drain lines in response to a scan signal from corresponding one of gate lines, wherein the signal stored in storage capacitor is supplied to display element (See Fig. 1A, items 2, 5, 8, from Col. 9, Line 38 to Col. 10, Line 35).

It would have been obvious to one ordinary skill in the art at time of the invention to incorporate teaching of Akiyama et al. into Okumura et al. system in order to reduce the power consumption (See Col. 3, Lines 23-29).

As to claim 13, Okumura et al. teaches a display apparatus wherein storing circuit has a predetermined number of storing elements, number corresponding to the number of bits in digital image signal and signal selector selects a signal to be supplied to display element from among predetermined number of signals, number corresponding to the number of bits in digital image signal (See Fig. 27, item 531, in description See Col. 27, Lines 5-15).

As to claim 25, 37, Okumura et al. teaches a display apparatus, capable of displaying a still image (See Col. 12, Lines 19-34).

As to claims 16, Okumura et al. teaches a display apparatus, capable of displaying a still image (See Col. 12, Lines 19-34).

As to claim 17, Okumura et al. teaches a display apparatus wherein, after still image is written to each of plurality of display pixels as a digital image signal, operation of driving circuits for driving plurality of display pixels are stopped until a new digital image signal is written to the same display pixels (See in description See Col.12, Lines 12-15).

As to claims 21, Okumura et al. teaches a display circuit selector for selectively supplying an image signal from corresponding one of drain lines and display circuit selector is switched in response to a switching signal, which is common to a plurality of pixels (See Fig. 2B, 3, items 125, CEL, in description See Col. 13, Lines 60-67 and Col.14, Lines 1-6, See Fig. 8, 9, items 230a, 230b, 261, 274, 276, in description See Col. 18, Lines 18-21 and 33-36).

As to claim 20, Okumura teaches a display apparatus comprising:

a plurality of gate lines provided in one direction of a substrate (See Fig. 2B, items La1, La2..., Col. 12, Lines 52-53);

a plurality of drain lines provided in a direction intersecting with gate lines (See Fig. 2B, items Lb1, Lb2..., Col. 12, Lines 52-53); and

a plurality of display pixels, each of which is selected by a scan signal supplied from corresponding one of plurality of gate lines, and which is supplied with an image signal from corresponding one of plurality of drain lines; wherein

each of plurality of display pixels comprises:

a display element (See Fig. 2B, 3, item CEL, Col. 13, Lines 16-24);

a first display circuit having a storing circuit, for storing a digital image signal from corresponding one of plurality of drain lines in response to a scan signal from corresponding one of gate lines (See Fig. 2B, 3, items Lai, Lbj, Col. 13, Lines 39-49).

Okumura et al. teaches the display signal may be stored in the first memory circuit in the either digital or analog form (See Fig. 27, items 532, 535, in description See Col. 27, lines 10-14 and Lines 51-55).

Okumura et al. does not show a second display circuit having a storage capacitor for storing an analog image signal from corresponding one of drain lines in response to a scan signal from corresponding one of plurality of gate lines.

Akiyama et al. teaches a display circuit having a storage capacitor for storing an analog image signal from corresponding one of drain lines in response to a scan signal from corresponding one of plurality of gate lines (See Fig. 1A, items 2, 5, 8, from Col. 9, Line 38 to Col. 10, Line 35).

It would have been obvious to one ordinary skill in the art at time of the invention to incorporate teaching of Akiyama et al. into Okumura et al. system in order to reduce the power consumption (See Col. 3, Lines 23-29).

As to claim 22, Okumura teaches a display apparatus comprising a plurality of display pixels, wherein each of display pixels comprises:

a pixel electrode (See Fig. 2B, 3, item CEL, Col. 13, Lines 16-24);

a first storing circuit, for storing a digital data and outputting signals to the pixel electrode (See Fig. 2B, 3, items CEL, Lai, Lbj, Col. 13, Lines 39-49

a storing circuit selector (See Fig. 3, item 123) for switching between first (See Fig. 3, item 121a) and second storing circuit (See Fig. 3, item 121b, Col. 14, Lines 7-54).

Okumura et al. teaches the display signal may be stored in the first memory circuit in the either digital or analog form (See Fig. 27, items 532, 535, in description See Col. 27, lines 10-14 and Lines 51-55).

Okumura et al. does not show a second storing circuit for storing analog data and outputting signals to pixel electrode.

Akiyama et al. teaches a second storing circuit for storing analog data and outputting signals to pixel electrode (See Fig. 1A, items 2, 5, 8, from Col. 9, Line 38 to Col. 10, Line 35).

It would have been obvious to one ordinary skill in the art at time of the invention to incorporate teaching of Akiyama et al. into Okumura et al. system in order to reduce the power consumption (See Col. 3, Lines 23-29).

As to claims 23, 35, Okumura et al. teaches a display apparatus wherein storing circuit has a predetermined number of storing elements, number corresponding to the number of bits in digital image signal and signal selector selects a signal to be supplied to display element from among predetermined number of signals, number corresponding to the number of bits in digital image signal (See Fig. 27, item 531, in description See Col. 27, Lines 5-14).

As to claims 26, 38 Okumura et al. teaches a display apparatus wherein, after still image is written to each of plurality of display pixels as a digital image signal, operation of driving circuits for driving plurality of display pixels are stopped until a new digital image signal is written to the same display pixels (See in description See Col.12, Lines 12-15).

As to claim 34, Okumura teaches a display apparatus comprising a plurality of display pixels, wherein each of display pixels comprises:

a pixel electrode (See Fig. 2B, 3, item CEL, Col. 13, Lines 16-24);

a first storing circuit, for storing a digital data (See Fig. 2B, 3, items CEL, Lai, Lbj, Col. 13, Lines 39-49

a memory selector (See Fig. 3, item 123) for switching a digital display mode in which first storing circuit is used in all of display pixels (See Fig. 3, item 121a) and second storing circuit (See Fig. 3, item 121b, Col. 14, Lines 7-54).

Okumura et al. does not show a second storing circuit for storing analog data and outputting signals to pixel electrode and an analog display mode in which second storing circuit is used in all of display pixels.

Akiyama et al. teaches a second storing circuit for storing analog data and outputting signals to pixel electrode (See Fig. 1A, items 2, 5, 8, from Col. 9, Line 38 to Col. 10, Line 35).

Since Okumura et al. teaches the display signal may be stored in the first memory circuit in the either digital or analog form (See Fig. 27, items 532, 535, in description See Col. 27, lines 10-14 and Lines 51-55), it would have been obvious to one ordinary skill in the art at time of the invention to incorporate teaching of Akiyama et al. into Okumura et al. system in order to reduce the power consumption (See Col. 3, Lines 23-29).

3. Claims 14, 24, 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al and Akiyama et al. as applied to claims 10, 22, 28, 36 above, and further in view of Sato et al. (US Patent No. 5, 712,652).

Okumura et al. and Akiyama et al. do not show storing circuit stores digital image signal using one or more inverters.

Sato et al. teaches how to use one or more inverters to store a digital image signal (See Fig. 1, items 4, 5, in description See Col. 9, Lines 43-46).

It would have been obvious to one ordinary skill in the art at time of the invention to replace one of memory circuit in the Okumura et al. and Akiyama et al. apparatus by the memory with one or more inverters as shown by Sato et al. in order to improve the storage capability and the image quality.

4. Claims 18-19, 27, 39 rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al, Akiyama et al. as aforementioned in claims 10, 22, 28, 34 in view of Hamada (EP 4144780).

Okumura et al, Akiyama et al. do not show a liquid crystal capacitor and a pair of electrodes for driving liquid crystal capacitor with individual display electrode for each display pixel and a facing electrode provided and at least one of the signals is an alternating current voltage signal oscillates around the voltage of facing electrode.

Hamada teaches how a reversed-phase a. c. voltage is applied to electrode b (See Fig. 4, items a, b, Vc and Vc', in description See Col.10, Lines 9-15).

It would have been obvious to one ordinary skill in the art at time of the invention to use alternating current as shown by Hamada and simple multiplexer in the Okumura et al, Akiyama et al. apparatus in order to display of clear, non-flickering constant image on the screen (See Abstract in the Hamada reference).

5. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al., Akiyama et al. as applied to claim 10 above, and further in view of Schleupen et al. (US Patent No. 5,517,543).

Okumura et al., Akiyama et al. do not show storing circuit stores digital image signal using one or inverters and a capacitor.

Schleupen et al. teaches to use capacitor and buffer amplifier to store image data. (See Fig. 1, items Tn1, Tn2 and Cn1, in description See Col. 4, Lines33-46).

It would have been obvious to one ordinary skill in the art at time of the invention to replace one of memory circuit in Okumura et al., Akiyama et al. apparatus by the holding capacitor and buffer amplifier as shown by Schleupen et al. to store digital image in order to order to improve the image quality.

6. Claims 28-29, 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al. in view of Akiyma et al. and Toyo (JP 58023091).

As to claim 28, Okumura et al. teaches a display apparatus comprising a plurality of display pixels, wherein each of display pixels comprises:

a pixel electrode (See Fig. 2B, 3, item CEL, Col. 13, Lines 16-24);

a first storing circuit, for storing a digital data (See Fig. 2B, 3, items CEL, Lai, Lbj, Col. 13, Lines 39-49);

a storing circuit selector (See Fig. 3, item 123) for switching between first (See Fig. 3, item 121a) and second storing circuit (See Fig. 3, item 121b, Col. 14, Lines 7-54).

Okumura et al. teaches the display signal may be stored in the first memory circuit in the either digital or analog form (See Fig. 27, items 532, 535, in description See Col. 27, lines 10-14 and Lines 51-55).

Okumura et al. does not show a second storing circuit for storing analog data and outputting signals to pixel electrode.

Akiyama et al. teaches a second storing circuit for storing analog data and outputting signals to pixel electrode (See Fig. 1A, items 2, 5, 8, from Col. 9, Line 38 to Col. 10, Line 35).

It would have been obvious to one ordinary skill in the art at time of the invention to incorporate teaching of Akiyama et al. into Okumura et al. system in order to reduce the power consumption (See Col. 3, Lines 23-29).

Okumura et al. and Akiyama et al. do not teach a signal selector for selecting a signal for display from among a plurality of signals based on an output of first storing circuit and for outputting the selected signal to pixel electrode.

Toyo teaches a signal selector for selecting a signal for display from among a plurality of signals based on an output of first storing circuit and for outputting the selected signal to pixel electrode (See Fig. 6-8, items 11-16, in description from page 6, last paragraph to page 8, 1st paragraph).

It would have been obvious to one ordinary skill in the art at time of the invention to incorporate teaching of Toyo into Akiyama et al. and Okumura et al. system in order to provide an image display device with low power consumption suitable for displaying still images (See page 5, 2nd paragraph in the Toyo reference).

As to claim 29 Okumura et al. teaches a display apparatus wherein storing circuit has a predetermined number of storing elements, number corresponding to the number of bits in digital image signal and signal selector selects a signal to be supplied to display element from among predetermined number of signals, number

corresponding to the number of bits in digital image signal (See Fig. 27, item 531, in description See Col. 27, Lines 5-14).

As to claim 31 Okumura et al. teaches a display apparatus, capable of displaying a still image (See Col. 12, Lines 19-34).

As to claim 32 Okumura et al. teaches a display apparatus wherein, after still image is written to each of plurality of display pixels as a digital image signal, operation of driving circuits for driving plurality of display pixels are stopped until a new digital image signal is written to the same display pixels (See in description See Col.12, Lines 12-15).

7. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al and Akiyama et al., Toyo as applied to claims 10, 22, 28, 36 above, and further in view of Sato et al. (US Patent No. 5, 712,652).

Okumura et al. and Akiyama et al., Toyo do not show storing circuit stores digital image signal using one or more inverters.

Sato et al. teaches how to use one or more inverters to store a digital image signal (See Fig. 1, items 4, 5, in description See Col. 9, Lines 43-46).

It would have been obvious to one ordinary skill in the art at time of the invention to replace one of memory circuit in the Okumura et al. and Akiyama et al., Toyo apparatus by the memory with one or more inverters as shown by Sato et al. in order to improve the storage capability and the image quality.

8. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al, Akiyama et al. and Toyo as aforementioned in claims 10, 22, 28, 34 in view of Hamada (EP 4144780).

Okumura et al, Akiyama et al. and Toyo do not show a liquid crystal capacitor and a pair of electrodes for driving liquid crystal capacitor with individual display electrode for each display pixel and a facing electrode provided and at least one of the signals is an alternating current voltage signal oscillates around the voltage of facing electrode.

Hamada teaches how a reversed-phase a. c. voltage is applied to electrode b (See Fig. 4, items a, b, Vc and Vc', in description See Col.10, Lines 9-15).

It would have been obvious to one ordinary skill in the art at time of the invention to use alternating current as shown by Hamada and simple multiplexer in the Okumura et al, Akiyama et al. and Toyo apparatus in order to display of clear, non-flickering constant image on the screen (See Abstract in the Hamada reference).

Response to Amendment

9. Applicant's arguments 05.14.04 filed on with respect to claims 10, 12-39 have been considered but are moot in view of the new ground(s) of rejection.

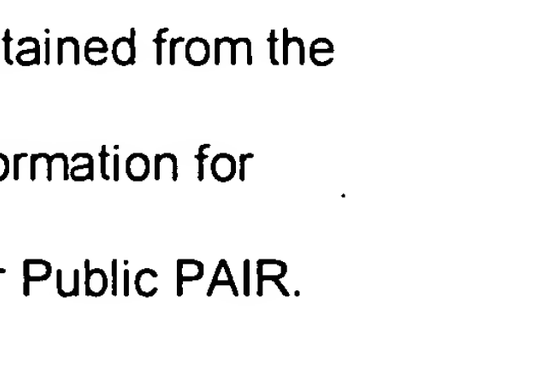
Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 703-305-5661. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ls 01.05.05



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